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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,916	06/07/2006	Hiroyuki Eguchi	062520	1487
38834 7590 07/24/2008 WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036				
EXAMINER BEHM, HARRY RAYMOND				
ART UNIT 2838		PAPER NUMBER		
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/581,916

**Applicant(s)**

EGUCHI ET AL.

**Examiner**

HARRY BEHM

**Art Unit**

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3 and 5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 March 2008 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_
- Paper No(s)/Mail Date \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to the amended claims have been considered but are largely moot in view of the new ground(s) of rejection. Examiner notes it is well known to compare a current value to a threshold to maintain the half period currents nearly equal; see for instance MacInnis (US 4,584,635).

"One of the prior art techniques involves sensing the current in each of the two switches directly and using the signal to control the switch turnoff signals. This technique is referred to as a current balancing or current mode technique. The current has a ramp or saw tooth waveform and it is compared to a reference voltage. The intention is to keep the switch currents equal and indirectly keep the DC component of the magnetizing current ( $I_m$ ) at 0." (MacInnis column 1, lines 40-49).

It is also well known to use a transformer turns ratio to step up or step down a voltage. The step up or step down turns ratio is adjusted to meet the load's voltage requirements and does not indicate a difficulty in implementing a particular turns ratio. See for instance Hulseley (US 5,568,026), which discloses a step up turns ratio where "The isolation transformer 30 has a predetermined step up turns ratio to increase the voltage and lower the current" (Hulseley column 2, lines 38-42).

Examiner also references Applicant's Background section in which the Admitted Prior Art of Figure 4 is described as performing "a step-up or step down operation". Examiner further notes for a bi-directional converter, a step down conversion becomes a step up conversion when the power flow is reversed.

***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, comparing the detected per-half cycle resonant current value to a threshold value, as in Claim 1, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain (US 6,519,168) in view of Jang (US 6,301,128) and Jansson (US 4,150,426).

With respect to Claim 1, Jain discloses a DC-AC converter comprising:

a transformer (Fig. 15 214) having primary side terminals (Fig. 15 102), secondary side terminals (Fig. 15 110), a primary side winding (Fig. 15 N1), and a secondary side winding (Fig. 15 N2);

a pair of switching means (Fig. 15 202-208) interposed between said primary side terminals and said primary side winding;

a LC resonant circuit (Fig. 15 Cs,Ls) comprised of a resonating reactor connected in series with said secondary side winding of said transformer, and a resonating capacitor that resonates with said resonating reactor;

a driving means (Fig. 5 502) for alternately turning said pair of switching means ON/OFF.

Jain does not disclose an output rectifier, but Jang discloses an output rectifier (Fig. 10 Controlled Full-Bridge Rectifier) for a bi-directional converter. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a

bi-directional DC-DC converter by implementing a full bridge rectifier in the secondary. The reason for doing so is to generate a DC output voltage "With the ability of the system to transfer power through the transformer in both directions, i.e., from the input to the output, and vice versa, the energy stored in the leakage inductances can be either transferred to the output, or the input, depending on the load requirement." (Jang column 3, lines 19-24).

Jain also does not disclose balancing the half cycle currents. Jansson discloses a converter with a resonant current detecting means (Fig. 1 7,8) for detecting a value per half cycle of the primary current; and

a current value comparing unit (Fig. 1 32,33) comparing the detected per-half cycle resonant current value to a threshold value (Fig. 1 31,30 output) and feeding the comparison result to said driving means are-provided; wherein

said driving means (Fig. 1 27,28) drives said pair of switching means by correcting their on-state lapses of time so that their on-state currents may be nearly equal ("substantially equalize the drive to the output transformer contributed by each output transistor", Jansson abstract) to each other based on the comparison result of said current value comparing unit. It would have been obvious to one of ordinary skill in the art at the time of the invention to balance the primary resonant current by comparing the primary currents to a threshold. The reason for doing so is "if the drive to each driver transistor is removed substantially at the instant at which the current in the main current path thereof reaches the value which the current in the main current path of the other said driver transistor had during the immediately preceding conduction period thereof,

the occurrence of saturation in the transformer can be at least delayed. If a current limit circuit is also provided to remove the drive to the driver transistors if the current in the main current paths thereof exceeds a certain amount, this delay may be sufficient to allow the current limit circuit to operate satisfactorily in all cases to prevent saturation from occurring in the transformer.” (Jansson column 2, lines 24-36).

With respect to Claim 2, Jain in view of Jang and Jansson disclose the DC-DC converter as set forth above, wherein said resonant current detecting means (Jansson Fig. 1 7) is provided on the primary side of said transformer.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain (US 6,519,168) in view of Jang (US 6,301,128), Jansson (US 4,150,426) and Hulsey (US 5,568,036).

With respect to Claim 3, Jain discloses a DC-AC converter comprising such known features as a transformer (Fig. 15 214), an LC resonant circuit (Fig. 15 Ls,Cs) on the secondary side, and driving means (Fig. 5 502) for driving a primary side full bridge inverter (Fig. 5 104).

Jain does not disclose boosting the output voltage, but Hulsey discloses a DC-DC converter stepping up the output of a bridge inverter (Fig. 1 21) with the turns ratio of transformer 30 and having low-voltage side terminals on the primary side, high-voltage side terminals on the secondary side, a low-voltage side winding on the primary,

and a high-voltage side winding on the secondary. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a step up turns ratio from the primary to the secondary and a low-voltage side pair of switching means interposed on the primary side between said low-voltage side terminals and said low-voltage side winding and a low-voltage side rectifying element [anti-parallel diode] connected in parallel with each of switching elements in said low-voltage side pair of switching means. The reason for doing so is to allow "for the use of a stepped-up voltage level" (Hulsey column 1, lines 55-57).

Jain also does not disclose an output rectifier, but Jang discloses an output rectifier (Fig. 10 Controlled Full-Bridge Rectifier) for a bi-directional converter. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a bi-directional DC-DC converter by implementing a full bridge rectifier (Fig. 10 Full Bridge Rectifier) having

- a high-voltage side pair of switching means (Fig. 10 S1-S4) interposed between said high-voltage side terminals and said high-voltage side winding;

- a high-voltage side rectifying element [anti-parallel diode] connected in parallel with each of switching elements in said high-voltage side pair of switching means;

- a driving means (Fig. 8 Driver, PWM Modulator) for turning ON/OFF the switching elements in said low-voltage side pair of switching means and the switching elements in said high-voltage side pair of switching means. The reason for doing so is to generate a DC output voltage "With the ability of the system to transfer power through the transformer in both directions, i.e., from the input to the output, and vice versa, the

energy stored in the leakage inductances can be either transferred to the output, or the input, depending on the load requirement.” (Jang column 3, lines 19-24).

Jain also does not disclose balancing the half cycle currents. Jansson discloses a converter with a resonant current detecting means (Fig. 1 7,8) for detecting a value per half cycle of the primary current; and

a current value comparing unit (Fig. 1 32,33) comparing the detected per-half cycle resonant current value to a threshold value (Fig. 1 31,30 output) and feeding the comparison result to said driving means are-provided; wherein

said driving means (Fig. 1 27,28) drives said pair of switching means by correcting their on-state lapses of time so that their on-state currents may be nearly equal (“substantially equalize the drive to the output transformer contributed by each output transistor”, Jansson abstract) to each other based on the comparison result of said current value comparing unit. It would have been obvious to one of ordinary skill in the art at the time of the invention to balance the primary resonant current by comparing the primary currents to a threshold. The reason for doing so is “if the drive to each driver transistor is removed substantially at the instant at which the current in the main current path thereof reaches the value which the current in the main current path of the other said driver transistor had during the immediately preceding conduction period thereof, the occurrence of saturation in the transformer can be at least delayed. If a current limit circuit is also provided to remove the drive to the driver transistors if the current in the main current paths thereof exceeds a certain amount, this delay may be sufficient to

allow the current limit circuit to operate satisfactorily in all cases to prevent saturation from occurring in the transformer.” (Jansson column 2, lines 24-36).

With respect to Claim 5, Jain in view of Jang, Jansson and Hulsey discloses the bi-directional DC-DC converter according to claim 3, wherein said low-voltage side pair of switching means (Jain Fig. 15 104) and said high-voltage pair of switching means (Jang Fig. 10 Controlled Full-Bridge Rectifier) are each configured by interconnecting four switching elements in a bridge.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pelligrino (US 4,477,867) and Deisch (US 4,148,097) disclose current balancing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HARRY BEHM whose telephone number is (571)272-8929. The examiner can normally be reached on 7:00 am - 3:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm E. Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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